A 1.9-GHz DECT CMOS Power Amplifier with Fully Integrated Multilayer LTCC Passives

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***Abstract*—We present the first demonstration of a CMOS power amplifier (PA) utilizing fully integrated multilayer low-temperature co-fired ceramic (LTCC) high-Q passives for 1.9-GHz digital European cordless telecommunications (DECT) applications. The inductor and capacitor library were built in a multilayer LTCC board using a compact topology. An inductor Q-factor as high as 100 with a self-resonant frequency (SRF) as high as 8 GHz was demonstrated. Measured results of the CMOS-LTCC PA show good agreement with the simulated results exhibiting 48% power added efficiency, 26-dBm output power and 17-dB gain at 1.9 GHz with a 3.3-V drain supply voltage. This result is the first significant step toward a compact DECT transceiver module development utilizing fully integrated multilayer LTCC passives and a standard CMOS technology.**

I. Introduction

SIZE reduction and full integration are key trends in commercial RF component production. Recently, two-chip or three-chip solutions for 1.9-GHz digital European cordless telecommunications (DECT) applications have been presented based on various silicon-based technologies [1]–[3]. These chips need to be integrated with off-chip filters and discrete passive elements, such as chip inductors and capacitors, to build a complete RF transceiver module. A single-chip solution for a partial functional block is developed for DECT applications based on a commercial BiCMOS technology [4]. However, it still requires integration with a power amplifier, a low-noise amplifier, and filters. A major bottleneck hindering full integration onto a single chip using standard CMOS technologies is the fact that the on-chip passives, such as inductors, capacitors and filters, require high-Q values. Multilayer low-temperature co-fired ceramic (LTCC) is one of the compact and cost-effective solutions to this problem. It is attractive to implement a complete RF transceiver module based on a standard silicon technology with LTCC passives in order to replace low-Q passives on silicon [5] with multilayer high-Q passives such as inductors [6] and filters [7], [8]. This fact demonstrates that the LTCC is a good candidate for system-on-package (SOP) solutions [9].

In this letter, we show the result of the first reported MOSFET power amplifier (PA) with fully integrated multilayer LTCC passives, suitable for 1.9-GHz wireless communication systems using constant envelope modulation schemes. We developed the LTCC inductor and capacitor library that allows high-Q passives and a higher level of integration in addition to eliminating the assembly time and cost incurred by the discrete off-chip components. The inductor components in the library were implemented using multilevel ground plane architecture to allow for a compact realization. The capacitors used for matching and RF ground utilize the vertically interdigitated configuration (VIC) and the conventional metal-insulator-metal (MIM) topology. The LTCC passives were simulated using a commercial electromagnetic simulator [10] and represented as an equivalent circuit model. For implementing a high-performance power amplifier, a custom nonlinear MOSFET model [11] has also been developed and incorporated into a harmonic balance simulator.

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II. LTCC Passive Library

The power amplifier was built using Dupont's 20-layer 951AT-based LTCC passive component library. The ceramic tape thickness is 3.6 mil with 7-μm silver or gold metallization on the surface layer and silver metallization for the buried layers. The LTCC inductor library was built based on the multilevel ground plane concept that allows for a considerable savings in real estate by maintaining the lateral size of the inductor footprint while varying the values of inductance. All of the inductor footprints are on the surface layer in microstrip configurations with buried ground planes. Various effective inductances $(L_{\rm eff})$ can be obtained by changing the shunt parasitic capacitance $(C_{\rm s})$ to ground. The inset of Fig. 1 shows the topology of the LTCC inductors. Moving the ground plane closer to the inductor footprint increases $C_{\rm s}$, thereby canceling part of the inductance. On the other hand, moving the ground plane farther from the structure reduces $C_{\rm s}$ and increases $L_{\rm eff}$. Fig. 1 shows the measured Q of the inductors used in the power amplifier circuit showing Q of two single-turn circular inductors with a line width of 10 mils, a diameter of 54 mils, and h_1 and h_2 of 7.2 mils and 21.6 mils, respectively. A Q-factor as high as 100 with the corresponding self-resonant frequency (SRF) of 8 GHz was obtained for the 1.4-nH inductor.

The capacitor library was built using a compact topology termed the VIC and MIM configurations. The concept of the VIC structure is shown in Fig. 2. This structure implements a capacitor by stacking and intertwining electrodes in a multilevel dielectric system. Such a configuration is suitable for realizing a large capacitance, such as the RF ground capacitor, in a multilayer board. Stacking and intertwining multiple electrodes is equivalent to establishing parallel capacitor interconnects whose total capacitance is the sum of the individual capac-

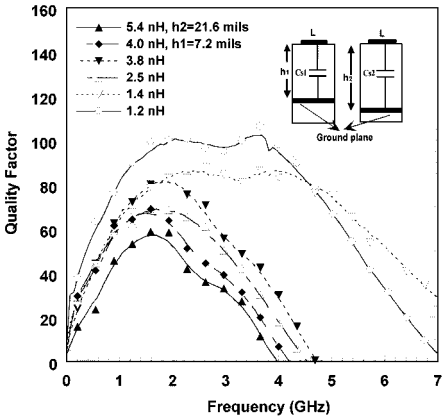

Fig. 1. Measured Q of the inductors based on the multilevel ground plane concept in the power amplifier module implementation. The inset shows the topology of the LTCC inductors. C_s is shunt parasitic capacitance between the inductor footprint and ground plane.

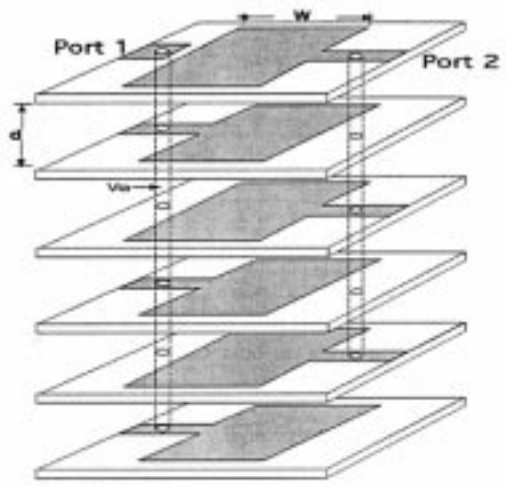

Fig. 2. Illustration of a vertically interdigitated capacitor (VIC) topology in the LTCC board. This compact structure implements a capacitor by stacking and intertwining electrodes in a multilevel dielectric system.

itance formed by a pair of electrodes, as illustrated in Fig. 2. The VIC in the multilayer LTCC board has demonstrated the reduction of the area by almost an order of magnitude as compared to the MIM counterpart for the same effective capacitance with similar performance in terms of Q-factor and SRF. Table I shows a comparison between the VIC and MIM structures for the same nominal capacitance value. Five pairs of MIM were stacked to form the VIC's whose results are summarized in Table I. In addition to the passive library, a custom RF/microwave nonlinear MOSFET model for large signal applications has also been developed for the power amplifier design and demonstrates compatibility with standard commercial wireless CAD tools [11]. The complete large signal model was implemented in a harmonic balance simulator and incorporated in the high-efficiency CMOS-LTCC power amplifier simulation.

III. CMOS-LTCC Power Amplifier Design and Results

A two-stage 1.9-GHz DECT power amplifier with second-harmonic tuning circuits using silicon N-MOSFET's has been built utilizing the LTCC library. Fig. 3 shows the

TABLE I
Performance Comparison Between a Parallel Plate Capacitor (MIM) and a Compact Vertically Interdigitated Capacitor (VIC)

Type	C_{eff} (pF)	Plate Size (mil x mil)	Self Resonance Frequency (GHz)	Quality Factor at 1.9 GHz
Parallel Plate Capacitor	1.4 pF	45	6.8	59
Vertical Interdigitated Capacitor	1.4 pF	18	5.5	55

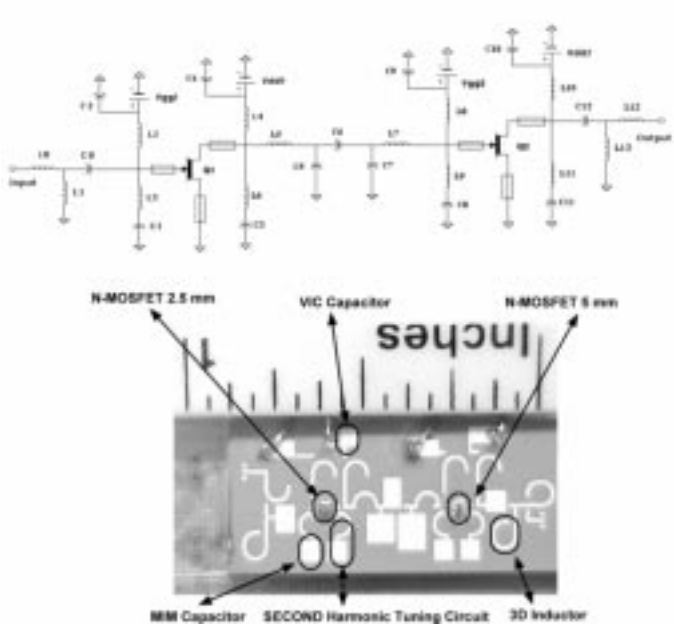

Fig. 3. Schematic diagram of the 1.9 GHz MOSFET-LTCC power amplifier (top) and photograph of the power amplifier module with NMOS devices wire bonded on the LTCC board (bottom).

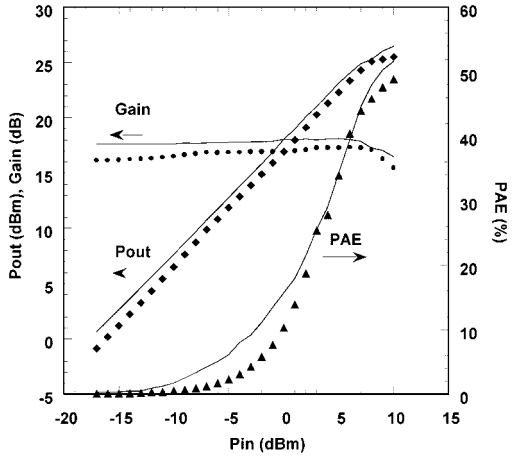

Fig. 4. Measured (▲, ♦, •) and simulated (solid line) gain, PAE, and output power of the CMOS-LTCC PA at 1.9 GHz with a 3.3-V drain supply voltage with class AB bias points (20% of $I_{\max}$).

schematic diagram and photograph of the LTCC power amplifier, which is designed to operate from a single 3.3-V supply. A single-ended, two-stage common source amplifier is implemented with an integrated reactive matching network using multilayer LTCC passives. For the high-efficiency operation, each stage of the PA was class AB biased (20% of

TABLE II
PERFORMANCE SUMMARY OF THE HIGH EFFICIENCY CMOS-LTCC POWER AMPLIFIER AT 1.9 GHz WITH A 3.3-V DRAIN SUPPLY VOLTAGE. THE HARMONICS DATA ARE MEASURED AT ONE dB COMPRESSION POINT OF OUTPUT POWER

Specification	Simulation Data	Measured Data
Frequency Range	1.88 GHz to 1.9 GHz	1.88 GHz to 1.9 GHz
Supply Voltage	3.3 V	3.3 V
Maximum Pout	27 dBm	26 dBm
Input VSWR	<1.5:1	<1.5:1
Gain Variation In Band	<0.5 dB	<0.8 dB
Harmonics	-38 dBc	-35 dBc
Power Added Efficiency	51 %	48 %
Power Gain	18 dB	17 dB

$I_{\max}$) incorporating second-harmonic tuning circuits in the input and output of each stage. The two N-MOSFET devices fabricated in a conventional 0.8 μm BiCMOS technology [11] were wirebonded onto gold pads on the LTCC board, which is connected to the bottom metal through vias. Using multiple bond wires from the chip to the RF ground pad minimizes the effect of bond-wire inductance. The gate periphery of the first and second stage device is 2.5 mm (50 fingers) and 5 mm (100 fingers), respectively. The substrate, source, and ground node are tied together eliminating body bias effects. The size of these discrete power MOSFET's is $400\ \mu\text{m} \times 700\ \mu\text{m}$. To ensure that the driver stage does not enter saturation before the output stage, a slightly oversized transistor has been chosen for the first stage device. Half- and quarter-turn inductors were used as matching components, while a full-turn inductor was used for an RF choke. Parallel plate MIM capacitors were utilized as matching components for the fundamental signal since their values and sizes are relatively small. The RF ground capacitors were implemented in the compact VIC topology since they require large capacitance value for 1.9-GHz applications. Second-harmonic tuning elements were implemented through a series LC resonator at 3.8 GHz as part of the second-harmonic trap network to improve the efficiency.

Fig. 4 shows the measured gain, PAE, and output power of the fabricated CMOS-LTCC PA at 1.9 GHz, demonstrating a good correlation to the simulated results performed using the LTCC passive library and the custom-developed MOSFET nonlinear model [11]. The power amplifier exhibits 48% PAE, 26-dBm output power, and 17-dB power gain at 1.9 GHz with a 3.3-V drain supply voltage, as indicated in Fig. 4. The measured second- and third-harmonics are lesser than -35 dBc at one dB compression point (P1dB) due to the second-harmonic traps and a low pass filter topology of the output matching circuit for the second stage. Table II provides a detailed summary on the measured and simulated power amplifier performance. This CMOS-LTCC module with multilayer integral passives can be used in the development of other RF transceiver modules for 1.9-GHz wireless communication applications that employ a constant envelope modulation scheme.

IV. CONCLUSION

We report the first demonstration of a 1.9-GHz CMOS power amplifier module with fully integrated high-Q LTCC passives. Under a low drain supply of 3.3 V, a PAE of 48%, an output power of 26 dBm, and an associated gain of 17 dB were obtained at 1.9-GHz. This is a significant step toward a higher level of integration for complete, compact, and cost-effective 1.9-GHz DECT transceiver module developments based on a standard MOSFET technology and fully integrated high-Q multilayer LTCC passives. This technology is applicable to other 1.9-GHz transceiver module development with a constant envelope modulation scheme.

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